APPENDIX A

"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

SPECIFICATION:

Replacement for the paragraph beginning at page 2, line 22:

a1

The present invention seeks to solve the problems associated with the prior art described above. It is an object of the present invention to provide a video data transfer system that increases the capturing rate of video data to be sent to the system memory.

Replacement for the paragraph beginning at page 6, line 1:

Then, the system checks the video data if it may be transferred to the system bus 17 (step 110). If the video data may be transferred, it is transferred to the system bus 17 and stored in the system memory 18 (step 111). If, in step 110, the system determines that the video data may not be transferred to the system bus 17 for some reason, the system checks the vertical synchronization signal data to see if the video data is the last part of a field (step 112). If the video data is not the last part of a field, the system transfers the next data to the FIFO memory 24 (steps 108 and 109); if the video data is the last part of a field, the system closes the gate 23 to stop data transfer and suspends frame capturing (step 113).

a2

Replacement for the paragraph beginning at page 7, line 19:

a3

On the other hand, the capturing-only path 26 comprises the gate 23 that enables/disables the FIFO memory 24, and the 32-bit-by-640-stage (YUV 16 bits, 2 lines of video data) FIFO memory 24.

CLAIMS (with indication of amended or new):

sub B5

1. (Amended) A video data transfer system comprising:

a real time output path through which video data processed by a video processor is sent to a display via a frame buffer;

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a capturing-only path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus; and

a gate in said capturing-only path, said gate being controllable to permit said video data to pass when received from said video processor.

2. (Amended) A video data transfer system, comprising:

a real time output path through which video data processed by a video processor is sent to a display via a frame buffer;

a capturing-only path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus, wherein

said real time output path comprises:

an off-screen memory which receives video data from said video processor via a data bus and stores video data therein, said off-screen memory being in the frame buffer; and

a display control circuit which receives video data read from said off-screen memory via said data bus for enlargement and interpolation processing and transfers processed results to said display, and wherein

said capturing-only path comprises:

a gate which is opened only when video data is received from said video processor for capturing; and

memory means for storing said video data sent through said gate and for transferring said video ~~data to said system bus.~~

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4. (New) A video data transfer system as defined in claim 1, further comprising:

a capture path memory in said capturing-only path;

said capture path memory being connected to said gate; and

said capture path memory being operable to store said video data passed by said gate.

5. (New) A video data transfer system as defined in claim 4, wherein said capture path memory is further effective to transfer said video data to said system bus.

6. (New) A video data transfer system as defined in claim 5, wherein said real time output path further comprises:

an off-screen memory effective to receive said video data from said video processor via a data bus and stores said video data therein; and

said off-screen memory being in said frame buffer.

7. (New) A video data transfer method, comprising:

providing video data from a video processor to a plurality of paths independent of each other;

sending said video data to a display through a frame buffer in at least one of said independent paths operating as a real time output path;

sending said video data to a system memory through a system bus in at least another of said independent paths operating as a capture-only path; and

controlling said capture-only path to permit said video data to pass to said system memory when said video data is to be captured.

8. (New) A video data transfer method as defined in claim 7, further comprising storing said video data in a capture path memory in said capture-only path when said video data is permitted to pass to said system memory.

9. (New) A video data transfer method as defined in claim 8, further comprising checking said system bus for occupation by other devices connected thereto.

10. (New) A video data transfer method as defined in claim 9, further comprising transferring said video data from said capture path memory to said system memory when said system bus is not occupied by other devices connected thereto.

11. (New) A video data transfer method as defined in claim 10, further comprising checking said video data stored in said capture path memory for at least one of a field and a frame delimiter when said system bus is occupied.

12. (New) A video data transfer method as defined in claim 11, further comprising controlling said capture-only path to prevent said video data from being stored in said capture path memory when said capture path memory contains said at least one of a field and a frame delimiter.

APPENDIX C

"CLEAN" VERSION OF EACH CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

1. A video data transfer system comprising:

a real time output path through which video data processed by a video processor is sent to a display via a frame buffer;

a capturing-only path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus; and

a gate in said capturing-only path, said gate being controllable to permit said video data to pass when received from said video processor.

2. A video data transfer system, comprising:

a real time output path through which video data processed by a video processor is sent to a display via a frame buffer;

a capturing-only path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus, wherein

said real time output path comprises:

an off-screen memory which receives video data from said video processor via a data bus and stores video data therein, said off-screen memory being in the frame buffer; and

a display control circuit which receives video data read from said off-screen memory via said data bus for enlargement and interpolation processing and transfers processed results to said display, and wherein

said capturing-only path comprises:

a gate which is opened only when video data is received from said video processor for capturing; and

memory means for storing said video data sent through said gate and for transferring said video data to said system bus.

3. A video data transfer system as defined in claim 2, wherein

said memory means transfers said stored video data to said system bus when said system bus is not occupied by some other unit and, when said system bus is occupied by some other unit, checks if said stored data contains a field delimiter or a frame delimiter and closes said gate to stop data transfer

when said stored data contains the delimiter and, when said stored data does not contain the delimiter, stores the next video data passing through said gate.

4. A video data transfer system as defined in claim 1, further comprising:

a capture path memory in said capturing-only path;

said capture path memory being connected to said gate; and

said capture path memory being operable to store said video data passed by said gate.

5. A video data transfer system as defined in claim 4, wherein said capture path memory is further effective to transfer said video data to said system bus.

6. A video data transfer system as defined in claim 5, wherein said real time output path further comprises:

an off-screen memory effective to receive said video data from said video processor via a data bus and stores said video data therein; and

said off-screen memory being in said frame buffer.

7. A video data transfer method, comprising:

providing video data from a video processor to a plurality of paths independent of each other;

sending said video data to a display through a frame buffer in at least one of said independent paths operating as a real time output path;

sending said video data to a system memory through a system bus in at least another of said independent paths operating as a capture-only path; and

controlling said capture-only path to permit said video data to pass to said system memory when said video data is to be captured.

8. A video data transfer method as defined in claim 7, further comprising storing said video data in a capture path memory in said capture-only path when said video data is permitted to pass to said system memory.

9. A video data transfer method as defined in claim 8, further comprising checking said system bus for occupation by other devices connected thereto.

10. A video data transfer method as defined in claim 9, further comprising transferring said video data from said capture path memory to said system memory when said system bus is not occupied by other devices connected thereto.

11. A video data transfer method as defined in claim 10, further comprising checking said video data stored in said capture path memory for at least one of a field and a frame delimiter when said system bus is occupied.

12. A video data transfer method as defined in claim 11, further comprising controlling said capture-only path to prevent said video data from being stored in said capture path memory when said capture path memory contains said at least one of a field and a frame delimiter.